

THE INFORMATION ON THE ABOVE IS TRUE AND CORRECT TO THE BEST OF MY KNOWLEDGE AND BELIEF.

forming a second interlayer dielectric layer over the first interlayer dielectric layer and over the conductive material pattern;

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a tungsten layer by forming the tungsten layer on the

2. The method of claim 1, wherein the conductive material pattern comprises a conductive material selected from the group consisting of polysilicon, undoped silicon, doped silicon, tungsten silicide, and tungsten.

3. The method of claim 1, wherein the glue layer further comprises a stack structure of the CVD TiN layers alone or a stack structure of both the CVD TiN layer and a PVD TiN layer.

4. The method of claim 1, wherein the CVD TiN layer is deposited to a thickness of less than about 400Å by using a TDMAT, TDMET or TiCl₄ source.

5. The method of claim 4, wherein a plasma treatment is further performed during or after the deposition of the CVD TiN layer while using N₂ and H₂ gas either together or alone.

6. The method of claim 1, wherein the CVD TiN layer includes a Ti layer and a TiN layer.

7. The method of claim 1, wherein the step of

selectively removing the first and the second interlayer dielectric layers is performed by using a gas, ion or radical having a fluorine source as an etch source.

5 8. The method of claim 7, wherein the gas having a fluorine source includes CF_4 , CHF_3 , CH_2F_2 , C_2F_6 , C_2F_8 or C_5F_8 .

10 9. The method of claim 1, wherein the forming step forms the two contact holes to have a difference in depth between the first and the second contact holes of more than 7000Å.

15 10. A method of forming a contact for a semiconductor device, comprising the steps of:

forming a first interlayer dielectric layer on a silicon substrate;

20 forming a conductive material pattern on a portion of the first interlayer dielectric layer, wherein the conductive material pattern has a lower etch rate than the first interlayer dielectric layer;

forming a second interlayer dielectric layer over the first interlayer dielectric layer and over the conductive material pattern;

selectively and sequentially removing the second and the first interlayer dielectric layers so as to form first and second contact holes, wherein the second contact hole has a depth greater than the first contact hole, wherein
 5 the first contact hole exposes a portion of the conductive material pattern, and wherein the second contact hole exposes a portion of the silicon substrate;

forming at least one CVD TiN layer on the first and the second interlayer dielectric layers including over
 10 the first and the second contact holes; and

forming a tungsten layer on the CVD TiN layer so as to fill the first and the second contact holes.

11. The method of claim 10, wherein the conductive
 15 material pattern is made of a conductive material selected from the group consisting of polysilicon, undoped silicon, doped silicon, tungsten silicide, and tungsten.

20 12. The method of claim 10, further comprising the step of:

forming a PVD TiN layer after or before the step of forming the CVD TiN layer.

13. The method of claim 10, wherein the CVD TiN layer is deposited with a thickness of less than about 400Å by using a TDMAT, TDMET or TiCl₄ source.

5 14. The method of claim 13, wherein a plasma treatment is further performed during or after the deposition of the CVD TiN layer while using N₂ and H₂ gas either together or alone.

10 15. The method of claim 10, wherein the CVD TiN layer includes a Ti layer and a TiN layer.

16. The method of claim 10, wherein the step of selectively and sequentially removing the second and the
15 first interlayer dielectric layers is performed by using gas, ion or radical having a fluorine source as an etch source.

17. The method of claim 16, wherein the gas having
20 fluorine source includes CF₄, CHF₃, CH₂F₂, C₂F₆, C₂F₈ or C₅F₈.

18. The method of claim 10, wherein the removing step selectively removes the dielectric layers so as to

provide contact holes having a difference in depth between the first and the second contact holes of more than 7000Å.

5 19. The method of claim 10, further comprising the step of:

performing a rapid thermal annealing process or a tube annealing process after or before the step of forming the CVD TiN layer.

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